ABSTRACT OF THE INVENTION

An adder for use in summing two binary numbers in an arithmetic logic unit of a processor or the like is disclosed and claimed. The adder includes a sparse carry-merge circuit adapted to generate a first predetermined number of carries and a plurality of intermediate carry generators coupled to the sparse carry merge circuit and adapted to generate a second predetermined number of carry signals. The adder further includes a plurality of conditional sum generators coupled to the intermediate carry generators and to the sparse carry-merge circuit to provide the sum of the two binary numbers. The adder may also include a multiplexer recovery circuit that enables a single rail dynamic implementation of the adder core.